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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,454	02/11/2000	Naoki Soeda	F-9680	5175

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EXAMINER	
CHEN, TIANJIE	

ART UNIT	PAPER NUMBER
2652	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,454	SOEDA, NAOKI	
	Examiner	Art Unit	
	Tianjie Chen	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-10,12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) *14-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-10,12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Rejection (RCE)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 5-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al (JP 5-81846A) in view of Bemis (US 5,487,160).

With regard to claim 1, Takao et al shows a magnetic disk apparatus in Fig. 1 including: a disk enclosure 12-14, a first printed-circuit board 2a, which is paired with the disk enclosure, and a second printed-circuit board 2b, which is detachably connected to the first printed circuit board 2a via a cable 27 ([0044]; Figs. 6(a) and 6(b)) and is separated in structure from the first printed-circuit board 2a (Fig. 12); wherein the first printed-circuit board mounts circuits which have a first noise resistance property, and a circuit 24 which holds parameters unique to the disk enclosure ([0015]); and wherein the second printed circuit board 2b mounts circuits which have a second noise resistance property; wherein the second printed-circuit board 2b is detachably connectable to an upper system, and wherein the first printed circuit board includes recording/reproduction control circuit 7 (Fig. 1, [0014]) (This limitation has been cited in papers mailed on 02/26/2002, 08.26/2002, and 02/21/2003; respectively).

Takao does not explicitly show enclosures and the circuits on the second printed-circuit board includes a switch for selecting either of one of the first printed-

circuit boards connected to the second printed-circuit board and another of the first printed-circuit boards connected to the second printed-circuit board.

Bemis shows a magnetic disk apparatus wherein a plurality of disk enclosures (Drive A-E, Fig. 6) are included; and the circuits 400 (Fig. 6) on the second printed-circuit board includes a switch for selecting either of one of the first printed-circuit boards connected to the second printed-circuit board and another of the first printed-circuit boards connected to the second printed-circuit board.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to include a plurality of disk enclosures and the switch in Takao's device. The rationale is as follows: Tanaka shows a plurality of enclosures 2a in Fig. 12. Bemis teaches that an array of disk drives is currently used in persona; computer and has been available for years (Column 1, lines 13-18). It is also well known in the art at the time the invention was made that a popular personal computer at home has more than one disk drive. Therefore, it is notorious technology at the time the invention was made to implementing a second disk drive in to a disk apparatus. One of ordinary skill in the art would have been motivated to implement a second disk disclosure into the apparatus thus obtaining more approaches for storage of information. The added disclosure would include a first printed circuit board as taught by Takao. In such constructed device, there would be circuits on each of the plurality of first printed-circuit boards includes a recording/reproducing control circuit.

Takao et al does not show that the second noise resistance property is superior to the first noise resistance property.

Office Notice is taken: as shown in Takao the first printed-circuit includes a circuit reading signal from a disk and amplifying the signal and then converting it into a digital signal. The original signal read form the disk is on the order of tens of mv (10^{-2} Volts); therefore, the first noise resistance property could only resist a noise of millivolts (10^{-3} Volts). And the second printed-circuit board includes data processing circuit, which is generally having IC chips, which deals with digitized signal having amplitude of 3-5 volts; therefore, the second noise resistance property could resist a noise of hundreds of millivolts (10^{-1} Volts).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to find that the second noise resistance property is superior to the first noise resistance property. The rationale is as follows: the second noise resistance property could resist a noise of 10^{-1} Volts, which is superior to the first noise resistance property, which could only resist a noise of 10^{-3} Volts. With regard to claim 2, In Takao et al and Bemis's device, the circuit on each of first printed circuit boards includes recording/reproduction control circuit 7 ([0014]).

With regard to claim 3, Takao et al shows an apparatus as described above, but does not explicitly show that circuit board 2a has an analog/digital converter.

But Takao et al shows that signal is read from the head by circuit 7 (line 1 in [0014]) and delivered to a logic operation circuit 6 (line 2 in [0013]).

It would have been obvious to provide an analog/digital converter in circuit board 2a. The rationale is as follows: the logic operation circuit deals with digital signals, the signals read from the head are analog. Therefore, an analog/digital converter in 2a is a necessity to convert the analog signals from 7 into digital signals, then feeding it into the logic operation circuit 6 through the connectors 3a and 3b.

One of ordinary skill in the art would have been expecting an analog/digit converter in the circuit board 2a for feeding digit signals into the logic operation circuit.

With regard to claim 5, Takao et al further shows that the circuits on the second printed-circuit board include a processor 6 ([0013]).

With regard to claim 6, Takao et al further shows that the circuits on the second printed-circuit board include a spindle motor/voice coil motor control circuit ([0027]).

With regard to claim 7, Takao et al further shows that each of the first printed-circuit boards further mounts a connector, which inherits some degree of elasticity.

With regard to claim 8, Takao et al shows that the circuits on the second printed-circuit board include a spindle motor/voice coil motor control circuit ([0027]).

With regard to claim 9, Takao et al shows that the circuits on the second printed-circuit board further include a single processor 4 and 6 ([0030].

With regard to claim 10, Takao et al further shows that the circuits on the second printed-circuit board include an interface circuit 5 ([0030]) with an upper system.

With regard to claim 12, Takao et al shows that the circuits on the second printed-circuit board are separated into a third printed circuit board 5 and a fourth printed circuit 6; wherein the third printed circuit board mounts the interface control circuit 5 and wherein the fourth printed circuit board mounts the logic calculation circuits 6.

Takao et al does not show that the circuits on the fourth printed circuit board is better in noise resistance than the interference control circuit.

It would have been obvious at the time the invention was made to one of ordinary skill to expect that in Takao et al's device that the circuits on the fourth printed circuit board is better in noise resistance than the interference control circuit. The rationale is as follows: the interface control unit works with a current, which is much larger than the current in the logic operation circuit. And the logic operation circuit is much sensitive to the noise, because even a low level noise can cause miscalculation in the logic operation circuit. One of ordinary skill would have been motivated to make the fourth printed circuit board is better in noise resistance than the interference control circuit in order to ensure the logic operation circuit working properly.

Response to Arguments

- Applicant's traverse on Restriction was answered on Office action mailed on 10/01/2003 and the restriction has been made final therein. Applicant made an argument on Restriction issue on 01/30/2004 and was answered again in Office action mailed on 04/13/2004. Examiner sees no reason for continuously making such an argument.
- Applicant argues in Remark: "the combination would not teaches or suggest each and every element of claimed invention." However, Applicant does not specify which element has not been taught or suggested. Examiner asserts that every element has been addressed.
- Applicant's argument made on 12/19/2003 has been answered in Office action mailed on 04/13/2004; which are recited below:
    - As stated in the rejection, there is sufficient motivation for combining these two references: (1) Tanaka has shown two disclosures with two first

circuit boards already. (2) Using two disclosures within a device was already a notorious technique at the time the invention was made. In a commonly used personal computer, the second printed-circuit board is a disk driver control card which is detachable connectable to an upper system (the mother board). (3) Tanaka also shows that the second printed circuit board 2b is detachable connected to a plurality of first circuit boards 2a in Fig. 12.

- Applicant also argues some features, which are not recited in claims. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the features recited above) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

- Takao et al (JP 5-81846A) clearly shows that the first printed-circuit board includes a recording/reproducing control circuit 7 (Fig. 1, [0014]). This limitation was cited in papers mailed on 02/26/2002, 08.26/2002, and 02/21/2003; respectively.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tianjie Chen whose telephone number is (703) 305-7499. The examiner can normally be reached on 8:00-4:30, Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chen Tianjie

TIANJIE CHEN
PRIMARY EXAMINER 10/25/04